

IC Technologies for Mixed-Signal and RF SiP

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Today's analog systems (PCS, Bluetooth, WLAN) have turned to a mixed-signal System-in-Package (SiP) that requires specialty foundries providing advanced analog CMOS-based process technologies for better cost, performance, and time to market than a System-on-Chip (SoC). The SiP approach also offers an alternative to challenges involved with integrating analog and digital functions into an SoC design.

SiPs allow the system designer to implement the analog and digital partitions in different technologies optimized for those specific functions. The digital components can be integrated into advanced CMOS, while the analog and RF blocks can be implemented in CMOS or high performance SiGe BiCMOS. This is becoming increasingly important as larger sections and more functionality are integrated into RF and analog products.

The SiP design platform is widely used for digital systems, such as DRAM and Flash memories, that drive packaging and assembly technique innovation. SiPs and multi-chip packages (MCPs) are also prevalent in the analog front end (AFE) of many wireless systems for power amplifier modules using specialized IC technologies, expert user design tools, and customized assembly and packaging techniques to achieve the required system performance. As the number of SiP applications increases, the tools and techniques required for mixed-signal SiP design improve and now support high-volume manufacturing, including analog and mixed-signal products. This evolution provides designers with an alternative to the SoC approach by using system partitioning.

SiP partitioning provides an alternative to integrating high-performance analog blocks onto an SoC in an advanced digital process. In this approach, the RF IC technology is complementary to the advanced digital CMOS. Large digital blocks can be designed in a 90- or 65-nm digital CMOS process, while analog functions are optimized in low-cost,

high-performance specialty processes, including RF CMOS, HV CMOS or SiGe BiCMOS at larger geometries (180 nm). In addition to reducing the size and cost of the large digital CMOS, the SiP allows the designer to mix and match which process is best for each function.

A simplified example of SiP partitioning in a wireless system is shown in Figure 1. A typical handheld radio system includes analog/RF blocks such as the PA, LNA, VCO, PLL, and ADC in the analog partition. It also requires integrated passive devices and power management functions. The digital partition includes baseband processing, memory, camera processing, and other digital functions.

Applying the SiP design approach allows each of these partitions to be individually optimized, affords IP re-use, and reduces time-to-market. Using the optimal process technology for each system partition helps to realize these advantages.

Specialty Analog / RF Foundry Technology

Specialty foundries have been able to accelerate the adoption of mixed-signal/RF SiP by offering customized technologies tailored to analog and RF systems. These specialty processes give fabless companies access to an optimized technology portfolio, allowing them to compete with integrated device manufacturers (IDMs). Specialty foundries also offer technology complementary to standard digital foundries, effectively broadening the technology portfolio available to fabless IC companies.

Table 1 shows typical CMOS-based RFIC technologies offered by specialty foundries. In addition to scaling gate geometries to keep up with Moore's Law, specialty foundries provide a wide range of technologies well-suited for different applications at each lithography node. These specialty technologies allow for analog scaling of system functions that do not scale well in digital processes.

SiGe BiCMOS technology is used extensively for analog system partition because of cost and manufacturability with improved RF performance over standard CMOS. SiGe BiCMOS processes add high-performance SiGe bipolar transistors (HBT) to a standard

CMOS process for the low-noise and high-speed properties advantages of the SiGe HBT. These characteristics make SiGe BiCMOS ideal for mixed-signal applications like low-phase-noise VCOs and LNAs used in wireless communications systems. Also, with higher breakdown voltages in the SiGe HBT, better noise figures and output power could be achieved than in a comparable design in a 90-nm CMOS process. As an example, a SiGe BiCMOS LNA can realize additional gain at one third the current consumption and half the power of a CMOS LNA [1].

CMOS power amplifiers are becoming more prevalent in low power applications. RFCMOS and LDMOS specialty processes offer extended operating voltages in a low-cost technology for this application. Comparisons have demonstrated that 0.25- μm RFCMOS can out-perform 65- and 90-nm CMOS as a result of higher operating voltage and lower parasitic resistances [2].

Additional SiP functionality can be provided by specialty foundries high-voltage technologies like HVCMOS, which offer CMOS devices capable of 8-12 V, or Bipolar-CMOS-DMOS (BCD) with even higher operating voltages for power management and driver applications. This ensures that operation under critical high-power conditions can be achieved using an SiP with an optimized high-voltage process; versus an SoC approach using advanced digital CMOS, which may be unable to meet power requirements.

Another feature of specialty process technologies is the ability to effectively scale the analog IC area using high-density, on-chip passive devices. High density MIM capacitors, high-Q inductors, and triple n-well processes allow for more compact designs at high speeds with improved performance, smaller die size, and lower cost.

Specialty foundries also provide thick back-end metal processes with low resistance and capacitance to reduce on-chip inductor area by a factor of two. This can result in improved performance with a quality factor (Q) of >30 attainable on chip. High-density MIM capacitors have also been developed that double the capacitance-per-unit area, further reducing die size. Additional analog technology details are available in [3-4].

Table 1 also shows some of the high-performance RF passive element modules made available by specialty technologies

A modular technology approach allows each of these passive elements to be applied across all of the baseline technologies, so designers can mix and match with system requirements, and adapt to new system requirements quickly and without a costly re-spin of an entire SoC. To support this, specialty foundries also provide RF device models, substrate noise models, statistical simulation capabilities, and are able to integrate their IC design environment with packaging and system design tools.

RF SiP IC technology roadmap

In the future, IC technologies will need to continue to scale both the digital and analog features to keep pace with RF-system size and performance requirements.

Specialty foundries will have to continue to reduce feature sizes and provide additional modular technologies to minimize costs. They are already prototyping lower cost modules that can accommodate the requirements of future mixed-signal and RF SiP designs. The question of minimizing costs in advanced specialty technologies remains.

An example of advanced modular technology is a 130-nm SiGe BiCMOS technology with low-cost HBT devices. By reducing fabrication complexity, the HBT and CMOS can both be implemented with the same performance at significant cost savings. Next-generation systems will push the frequency range even higher in 77 GHz automotive sensing and 60 GHz wireless applications. Fortunately, specialty processes already provide SiGe HBT devices with sufficient performance, and work is continuing to improve low-cost technologies and passive devices to make these systems cost-effective.

Future analog integration can also further improve wireless PA designs by facilitating high-performance switches on SOI integrated with LDMOS to be combined in the design of a CMOS PA. In the CMOS or SiGe BiCMOS technology, this can be extended to

include the transceiver function, depending on the SiP partitioning. Integrated MEMS for high-Q filters will also increase the functionality and reduce SiP costs.

Implementing all of this analog IP in a mature, high-yielding process — rather than continually porting IP to the next-generation of advanced digital CMOS — will allow fabless companies and IDMs alike to take advantage of specialty foundry processes.

Conclusion

All of the analog puzzle pieces are available from specialty foundries that provide IC solutions for analog integration. This approach complements the advanced CMOS processes at 65- and 90- nm which are ideal for highly integrated digital functions. While these digital processes are capable of analog integration, they are not as cost-effective, or of comparable performance, as specialty CMOS processes in mixed-signal systems.

Using specialty foundries in the mixed-signal/RF SiP design approach can be a more cost-effective system solution than SoC in many wireless systems. It is becoming more widely used today because of the advances in the IC technologies, EDA tools, and assembly techniques.

References

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Table 1

Table 1.a		Specialty RFIC Technology Modules	
0.5 μm	CMOS, RF CMOS, LDMOS, BCD		
0.35 μm	60 GHz SiGe BiCMOS		
0.25 μm	CMOS, RF CMOS, HV CMOS		
180 nm	CMOS, RF CMOS, LDMOS, HV CMOS 90, 120, 200 GHz SiGe BiCMOS		
130 nm	CMOS, RF CMOS 100, 150, 200 GHz SiGe BiCMOS		
Table 1.b		High performance RF passive elements	
Device		Feature	
High Density MIM capacitor		5.6 fF/ μm^2	
High Q inductor (Q @ 2.4 GHz)		>30	
Inductor metal thickness		Up to 6.0 μm	

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