TowerJazz Analog Mixed-Signal Power Management IC Reference Flow

Cadence
Custom IC Design Flow Solutions
Outline

• Overview of Cadence Design Solutions

• Reference Flow
  – Major Mixed-Signal Reference Sub-Flows
  – Cadence Mixed-Signal Design Platforms
  – Analog Block Design Sub-Flows
    • Schematic Capture
    • Verification
    • Layout Implementation

• Reference Design Example
  – TS018 (180nm BCD) Bandgap Reference Design
  – Reference Design Kit (RDK)
Cadence at the core of product development
Cadence strategy
Build complete solutions for pressing challenges

Solution Offerings
- System Development
- Enterprise Verification
- Low Power
- Mixed Signal
- Advanced Node

Ecosystem
- Systems
- Foundry
- IP
- EDA Partners
- Standards
- Alliances

Product Offerings
- System Design
- Logic Design
- Analog / Custom
- Digital Implementation
- PCB and IC Package Design
- Signoff and Manufacturing

Service Offerings
- Design outsourcing
- Infrastructure outsourcing
- Design environment Enablement
- Methodology enhancement
- Hosted and managed design solutions
- Design fundamentals (Training)
Evolution of Mixed Signal Design

Technology Implications

Older Design

Physical hierarchy separates digital and analog

Latest Design

Digital and analog distributed throughout design
Virtuoso: The gold standard for mixed-signal ICs

- 1000s of customer tapeouts
- Trusted by leading foundries and IP providers
- Production-proven PDKs available for every foundry
- Deep knowledge and expansive expertise within engineering community
- Integrated digital verification and implementation

Virtuoso platform

- DESIGN
- VERIFY
- IMPLEMENT

Process design kits and SKILL

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Mixed-Signal Implementation Solution
Interoperability Technology

- Black-box methodology insufficient
- Common data base for design data and constraints
- Area, power, noise tradeoff during floorplanning

Virtuoso® (Custom)
Encounter® (Digital)

OpenAccess

- Concurrent analog and digital layout
- Full chip signoff covering AMS blocks
- Facilitate collaboration between analog and digital designers
Power Management IC Implementation Challenges

✔ Multiple Power Supply Voltage Domains
  - Need to avoid connection errors such as connection to the wrong power domain
  - Advanced low-power techniques are introducing new verification challenges

✔ High Voltage
  - Voltage-dependent design rules
  - Layout placement guidelines
  - Special devices and layout isolation structures

✔ High Power
  - Electromigration (EM) and Voltage drop analysis (IR) verification a must
  - Possible thermal issues
  - Possible reliability issues
IC61 Virtuoso IC Design Platform

Virtuoso Schematic Editor (VSE) Products and Features

VSE-L
Built on familiar foundation

VSE-XL
Enhanced with powerful assistants
IC61 Virtuoso Schematic Editor XL

Dockable Assistants

Design Navigator

Property Editor

Circuit Prospector

Constraint Manager
IC61 Virtuoso Simulation “Cockpit”

Virtuoso Analog Design Environment (ADE) Products and Features

ADE-L Entry-level exploration
  – Initial design development

ADE-XL Specification compliance
  – Extensive analysis and verification

ADE-GXL Extensive Analysis
  – Design finishing up to six sigma yield standards
  – Early parasitic exploration

Parasitic Estimation

Mismatch Analysis

Sensitivity Analysis

Global Optimization

Local Optimization

Sweeps and Corners

Fast waveform Visualization

Specification Generation

Monte Carlo

SiP support

6-sigma DFY

Multiple Testbenches

Matlab/Ocean Measure support

Ocean scripting

Parametric sweeps

3rd party simulator support

3rd party simulator support

Parametric sweeps

3rd party simulator support

Parametric sweeps
IC61 ADE L Simulation Cockpit
A new interactive user interface

- **Loaded Design**
- **New Icons**
- **Parameterized Stop Freq**
- **Edit Variables here**
- **Status bar during simulation**
- **Loaded State**
Increase Quality and Test Coverage with:
A Single Analysis Environment – ADE XL

Setup & manage Multiple tests

Setup Signals to plot, Measures etc

Results summary

Sweeps
Corners
Monte Carlo
Parallelized Simulation
Documentation
Extensive Analysis and further productivity with:

Virtuoso ADE GXL

- Automate design centering
  - Find the optimum power/speed
  - Maximize yield up to 6 sigma

- Well integrated parasitic analysis
  - Explore parasitic effects early
  - Reduce iterations through Layout

- Assist key parts of the design flow
  - Behavioral model calibration to SPICE accuracy
    - Calibrate VerilogA, AMS or Liberty
Powerful Layout Creation and Editing
Virtuoso Layout Suite (VLS)

- **VLS L**
  
  *Foundation Layout Editing*
  
  - Layout entry, built on a common user interface and infrastructure

- **VLS XL**
  
  *Designer productivity through assisted automation*
  
  - Connectivity, constraint & design rule driven layout

- **VLS GXL**
  
  *Designer Productivity through full automation*
  
  - Full placement, routing, device generation, and optimization automation
Unified Design Constraint System
Adding Constraints to the Schematic

Old Method
Designer notes added to the schematic

New Method
Captured in Constraint System
Tracked and Enforced throughout the Design Flow

Constraint Types:
- Electrical
- Placement
- Routing
Unified Design Constraint System
Assisted Constraint Creation using the VSE
The Circuit Prospector

Design Navigator
Circuit Prospector
Circuit Finders
Grouped Results

Prospector Finder Results Highlighted on Canvas
Constraint Creation Button
Virtuoso Platform Integrated Design
GXL Level: Automated level of design creation

- VLS-GXL inherits the functionality of VLS-L and VLS-XL
  - Adds tokened plug-ins to run advanced & automated tasks
    - Floorplanning
    - Cell Planning
    - Modgens
    - Analog/Custom Placer
    - Custom Digital Placer
    - Block Placer
    - Virtuoso Space Based Router (VSR)
    - Virtuoso Chip Assembly Router (VCAR)
    - Virtuoso Layout Migrate (VLM)
Analog/Power Management Specific Features
Adding Guard Rings

Assisted Using Multipart Paths

Automated Using Guardring Utility
Custom IC Flow Solutions
BGR Reference Design Database (RDK)

Overview
BGR Reference Design Kit (RDK) Overview

- Used to Demonstrate the TowerJazz AMS Reference Flow
- Flow Validation Vehicle
- Version 1.0 Available for Download Soon
  - Available for download from TowerJazz Web Site for Qualified Customers
- TowerJazz-Supplied IP Block
  - Band Gap Reference Block
  - Based on the TS018 180nm Power Management Enabled BCD Process
- Portability
  - 100% Cadence Virtuoso-Based Flow
  - No External Library Dependencies
  - Only Specific Environment and Tool Configuration Dependencies
- Includes
  - Intermediate and Final Design Files
  - Simulation Testbenches and Results
  - Verification Run Scripts (Assura and QRC)
- Workshops Covering Complete Analog Block Design and Implementation Flows to be Available end of Q410
Reference Design Database (RDK) Structure

DESIGNS
  --
  TS018
  BGR
  --
  oa
  --
  BGR_IP

GPDK180
  --
  doc
  --
  spectre
  --
  gds

TECH
  --
  TS018
  --
  ts018_v1.1
  --
  oa
  --
  ts018_pm_prim

  --
  spectre

WORK
  --
  custom

  bin
  doc
  etc
  setup

User Workarea

README.txt

Makefile

cds.lib
common.lib
assura_tech.lib
cdsinit
project.cshrc

Reference Design Specific Files

TowerJazz ts018 PDK Files (Flow Enablement)

User workspace – tools generally launched from here – contains environment setup files
BGR Top-Level Schematics
BGR Top-Level Layout
TowerJazz RDK
Complete AMS Reference Flow
## Cadence Product Requirements

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Release</th>
<th>Release Type</th>
<th>Key Product Features</th>
<th>Tasks</th>
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</thead>
<tbody>
<tr>
<td><strong>Virtuoso (IC)</strong></td>
<td>6.1.4</td>
<td>Update</td>
<td>VSE XL ADE GXL VLS GXL</td>
<td>Schematic capture Simulation environment Layout design</td>
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<tr>
<td><strong>Assura</strong></td>
<td>41USR1OA_614</td>
<td>Update</td>
<td>Assura</td>
<td>DRC, LVS</td>
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<td><strong>EXT</strong></td>
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<td>Update</td>
<td>QRC</td>
<td>RC Extraction</td>
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<tr>
<td><strong>MMSIM</strong></td>
<td>7.2</td>
<td>Base</td>
<td>Spectre</td>
<td>Circuit Simulation</td>
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# TowerJazz RDK Release Schedule

<table>
<thead>
<tr>
<th>Q410</th>
<th>Q211</th>
<th>…</th>
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<tbody>
<tr>
<td><strong>Committed</strong></td>
<td><strong>Planned</strong></td>
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<tr>
<td><strong>AMS Flow v1.0</strong></td>
<td><strong>AMS Flow v2.0</strong></td>
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<tr>
<td><strong>Design:</strong> BGR</td>
<td><strong>Design:</strong> BGR</td>
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<tr>
<td><strong>Process:</strong> TS018</td>
<td><strong>Process:</strong> TS018</td>
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</tbody>
</table>

**Tools/BOM**
- IC 6.1.4
- ASSURA 4.1
- MMSIM 7.2
- EXT 9.1.1

**Flow/Database**
- AMS block
- AMS flow documentation
- Workshops

**v2.0 Planned Enhancements**
- Addition of Digital Block to Reference Design
- Demonstration of Encounter (EDI) Interoperability
- Mixed-Signal Simulation using AMSD/Ultrasim
- Virtuoso Power Solution (VPS) System
- IC6.1.5 Productivity Enhancement Features
Thank-You!
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